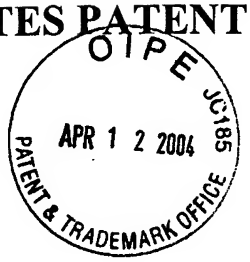
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re Application of :

Robert Stenberg
Ivan Pavisic

Serial No. :	10/083,411	**Group Art Unit :**	2825
Filed :	February 27, 2002	**Examiner :**	Do, Thuan
For :	Algorithm For Finding Timing Bottlenecks	**Atty Docket :**	72242 / 01-926

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Mark Salvatore

April 12, 2004 — Date

Mark Salvatore — Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milipitas, CA 95035
408-433-7475

Date: 4/8/04

Respectfully submitted,

Sandeep Jaggi

Reg. No. 43,331